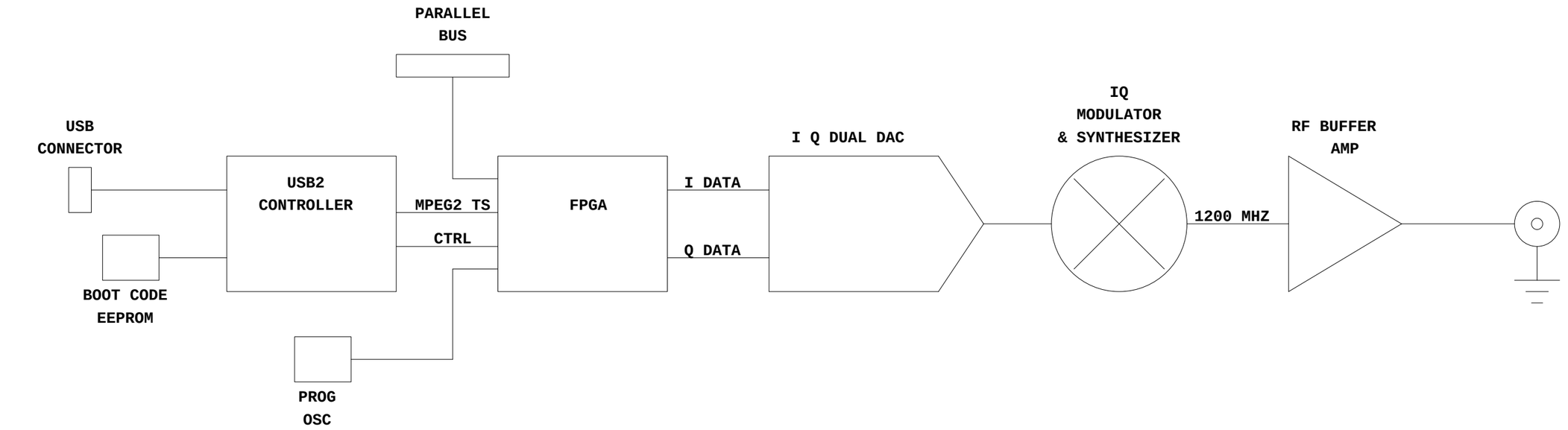
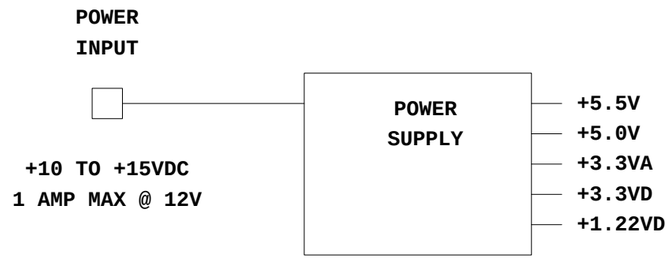
SHEET	DESCRIPTION
1	COVER SHEET AND BLOCK DIAGRAM
2	USB AND FPGA
3	DAC AND IQ MODULATOR/SYNTHESIZER
4	RF BUFFER AND CONNECTORS
5	POWER SUPPLIES
6	FPGA POWER, CONTROL AND DECOUPLING CAPACITORS

DATV EXPRESS

REVISION HISTORY





DATV Express

DATV Exciter

SCHEMATIC DIAGRAM,

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BLOCK DIAGRAM

CAD T. GOULD WB6P	
ENGR A. TOWSLEY WA8RMC	
MFG	
QC	
APVD	

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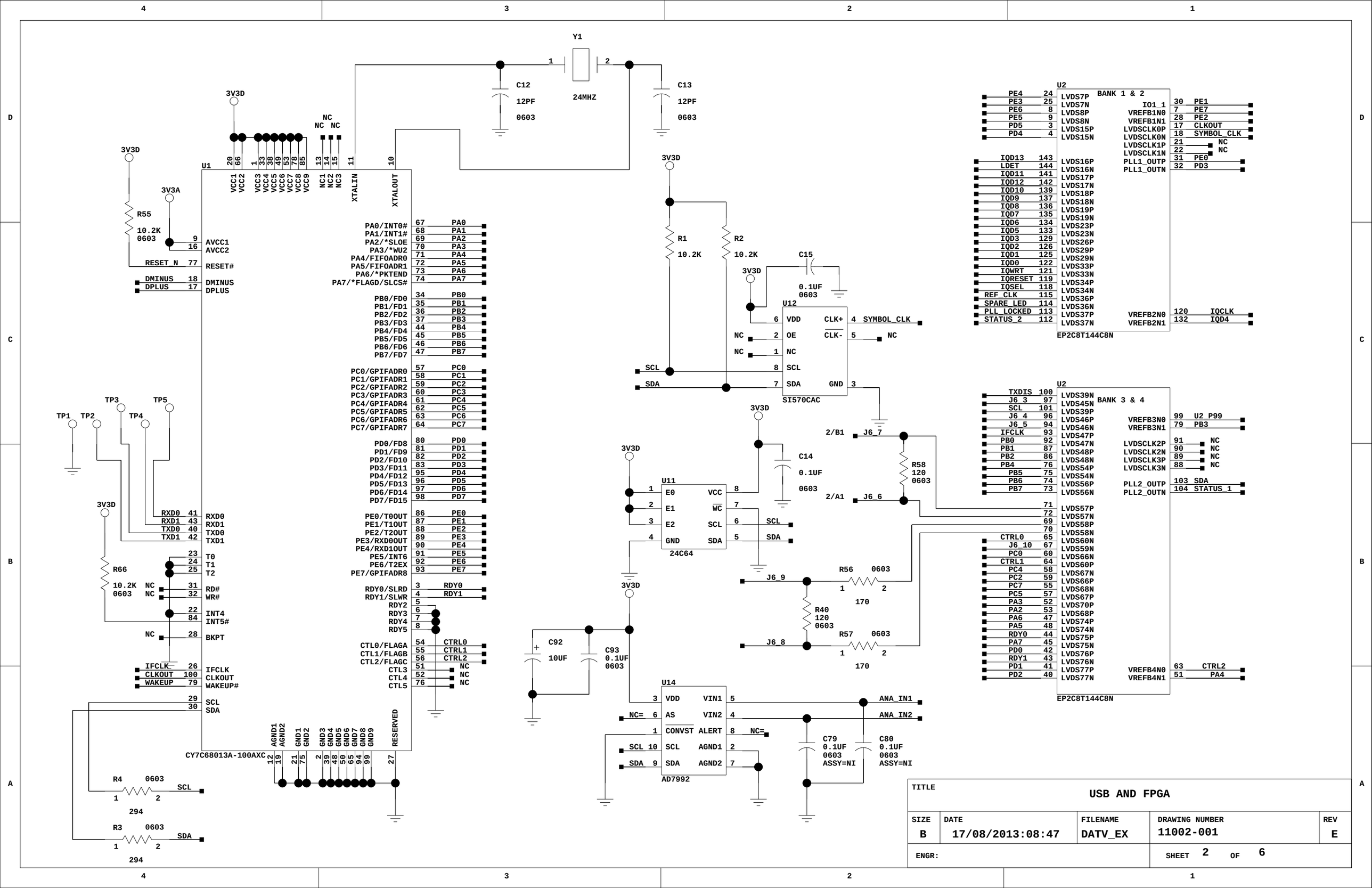
B	17/08/2013:08:47	DATV_EX	11002-001	E

ENGR:

SHEET 1 OF 6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24MHZ
C12
12PF
0603
C13
12PF
0603
3V3D
NC
NC NC
U1
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9
NC1 NC2 NC3
XTALIN
XTALOUT
3V3A
R55
10.2K
0603
AVCC1
AVCC2
RESET_N
RESET#
DMINUS
DPLUS
PA0/INT0# PA1/INT1# PA2/*SLOE PA3/*WU2 PA4/FIFOADR0 PA5/FIFOADR1 PA6/*PKTEND PA7/*FLAGD/SLCS#
PB0/FD0 PB1/FD1 PB2/FD2 PB3/FD3 PB4/FD4 PB5/FD5 PB6/FD6 PB7/FD7
PC0/GPIFADR0 PC1/GPIFADR1 PC2/GPIFADR2 PC3/GPIFADR3 PC4/GPIFADR4 PC5/GPIFADR5 PC6/GPIFADR6 PC7/GPIFADR7
PD0/FD8 PD1/FD9 PD2/FD10 PD3/FD11 PD4/FD12 PD5/FD13 PD6/FD14 PD7/FD15
PE0/T0OUT PE1/T1OUT PE2/T2OUT PE3/RXD0OUT PE4/RXD1OUT PE5/INT6 PE6/T2EX PE7/GPIFADR8
RDY0/SLRD RDY1/SLWR RDY2 RDY3 RDY4 RDY5
CTL0/FLAGA CTL1/FLAGB CTL2/FLAGC CTL3 CTL4 CTL5
TP1 TP2 TP3 TP4 TP5
RXD0 RXD1 TXD0 TXD1
T0 T1 T2
R66
10.2K
0603
RD# WR#
INT4 INT5#
BKPT
IFCLK CLKOUT WAKEUP
IFCLK CLKOUT WAKEUP#
SCL SDA
CY7C68013A-100AXC
AGND1 AGND2 GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 RESERVED
R4 0603 SCL
294
R3 0603 SDA
294
3V3D
R1
10.2K
R2
10.2K
C15
0.1UF
0603
U12
VDD CLK+ CLK- OE NC NC SCL SDA GND
SYMBOL_CLK
SI570CAC
2/B1 J6_7
2/A1 J6_6
R58
120
0603
U11
E0 E1 E2 GND VCC WC SCL SDA
24C64
C14
0.1UF
0603
J6_9 J6_8
R56 0603
170
R40
120
0603
R57 0603
170
C92
10UF
C93
0.1UF
0603
U14
VDD AS CONVST SCL SDA VIN1 VIN2 ALERT AGND1 AGND2
NC= NC= SCL SDA
AD7992
ANA_IN1 ANA_IN2
C79
0.1UF
0603
ASSY=NI
C80
0.1UF
0603
ASSY=NI
U2
BANK 1 & 2
PE4 PE3 PE6 PE5 PD5 PD4
IQD13 LDET IQD11 IQD12 IQD10 IQD9 IQD8 IQD7 IQD6 IQD5 IQD3 IQD2 IQD1 IQD0 IQWRT IQRESET IQSEL REF_CLK SPARE_LED PLL_LOCKED STATUS_2
LVDS7P LVDS7N LVDS8P LVDS8N LVDS15P LVDS15N LVDS16P LVDS16N LVDS17P LVDS17N LVDS18P LVDS18N LVDS19P LVDS19N LVDS23P LVDS23N LVDS26P LVDS29P LVDS29N LVDS33P LVDS33N LVDS34P LVDS34N LVDS36P LVDS36N LVDS37P LVDS37N
IO1_1 VREFB1N0 VREFB1N1 LVDSCLK0P LVDSCLK0N LVDSCLK1P LVDSCLK1N PLL1_OUTP PLL1_OUTN VREFB2N0 VREFB2N1
30 PE1 7 PE7 28 PE2 17 CLKOUT 18 SYMBOL_CLK 21 NC 22 NC 31 PE0 32 PD3 120 IQCLK 132 IQD4
EP2C8T144C8N
U2
BANK 3 & 4
TXDIS J6_3 SCL J6_4 J6_5 IFCLK PB0 PB1 PB2 PB4 PB5 PB6 PB7 CTRL0 J6_10 PC0 CTRL1 PC4 PC2 PC7 PC5 PA3 PA2 PA6 PA5 RDY0 PA7 PD0 RDY1 PD1 PD2
LVDS39N LVDS45N LVDS39P LVDS46P LVDS46N LVDS47P LVDS47N LVDS48P LVDS48N LVDS54P LVDS54N LVDS56P LVDS56N LVDS57P LVDS57N LVDS58P LVDS58N LVDS60N LVDS59N LVDS66N LVDS60P LVDS67N LVDS66P LVDS68N LVDS67P LVDS70P LVDS68P LVDS74P LVDS74N LVDS75P LVDS75N LVDS76P LVDS76N LVDS77P LVDS77N
VREFB3N0 VREFB3N1 LVDSCLK2P LVDSCLK2N LVDSCLK3P LVDSCLK3N PLL2_OUTP PLL2_OUTN VREFB4N0 VREFB4N1
99 U2_P99 79 PB3 91 NC 90 NC 89 NC 88 NC 103 SDA 104 STATUS_1 63 CTRL2 51 PA4
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USB AND FPGA
SIZE B
DATE 17/08/2013:08:47
FILENAME DATV_EX
DRAWING NUMBER 11002-001
REV E
ENGR:
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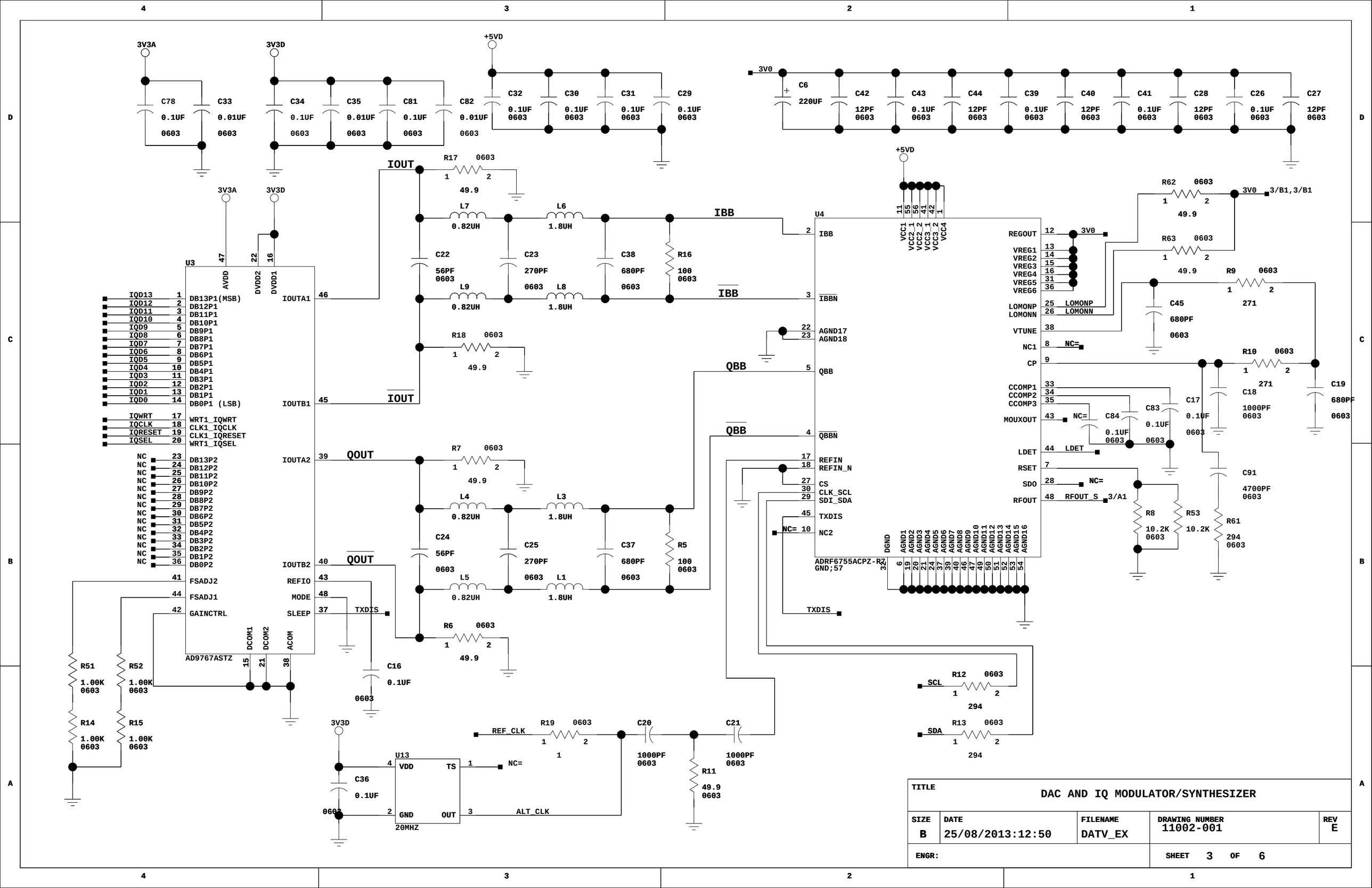

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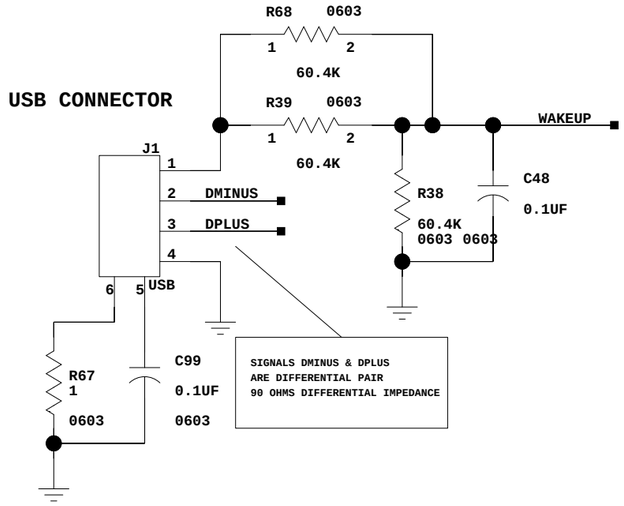
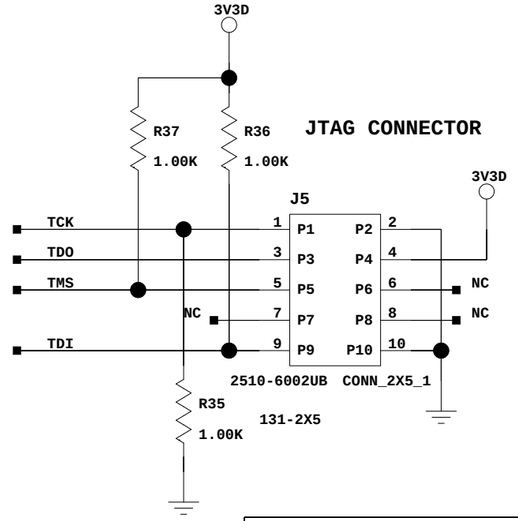
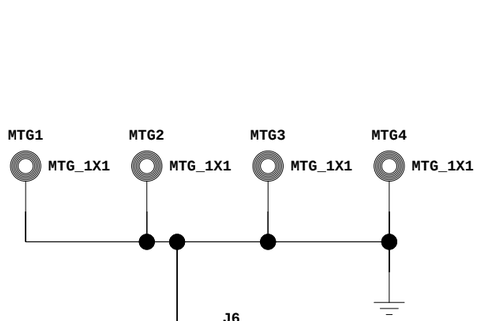
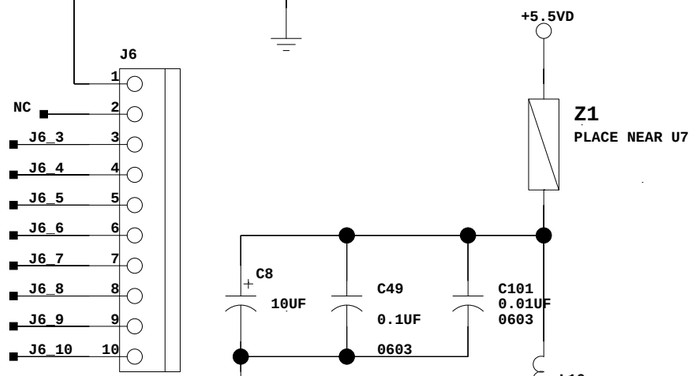
USB CONNECTOR

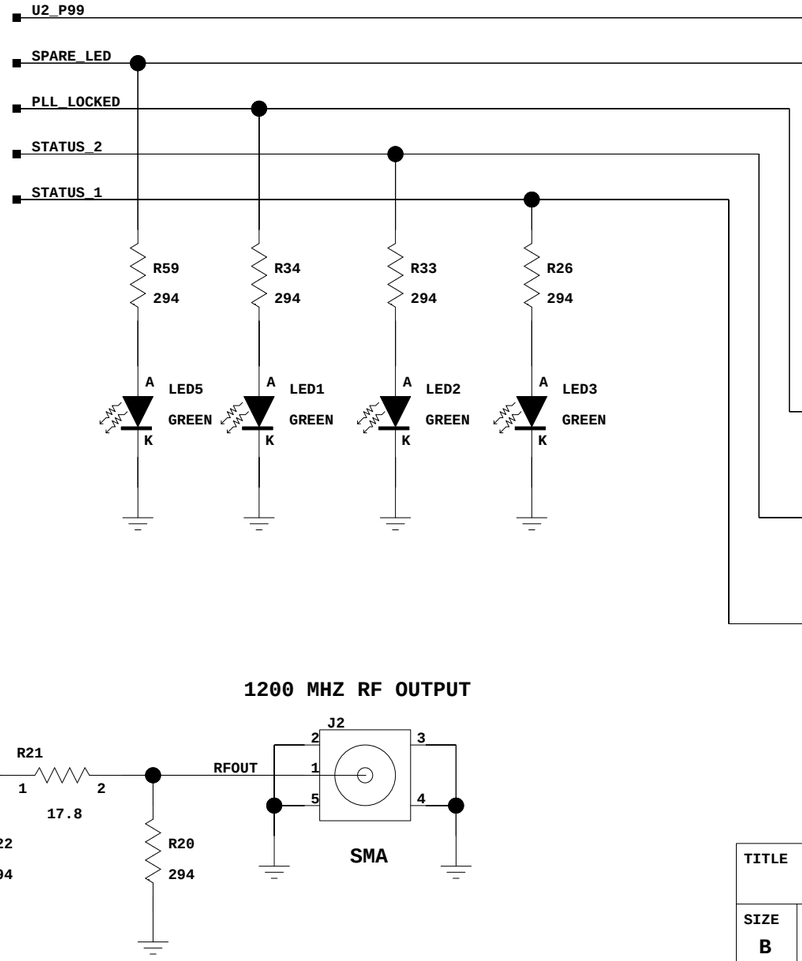


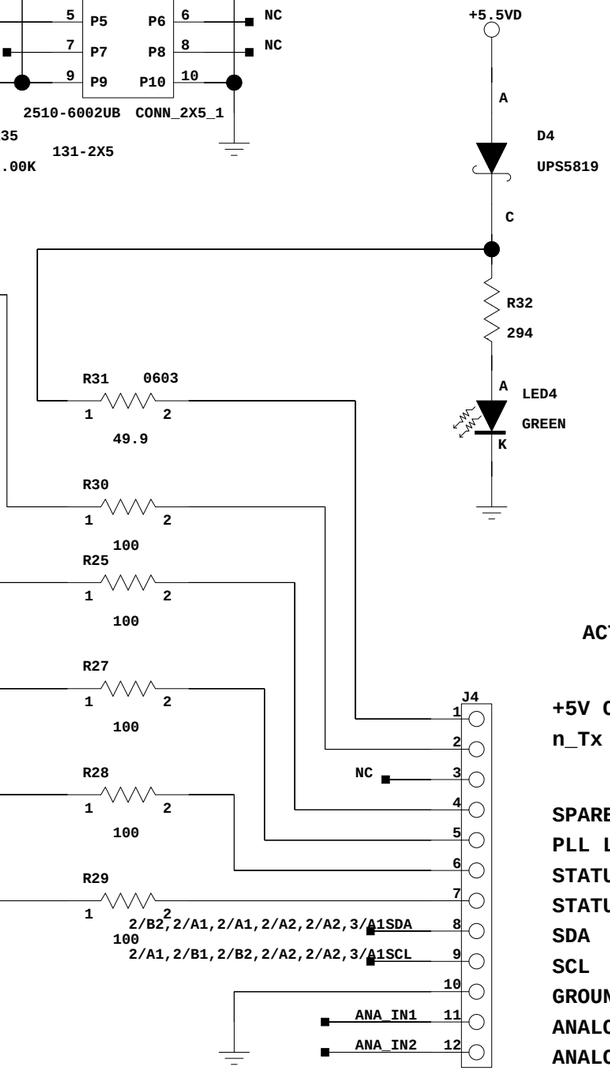
JTAG CONNECTOR

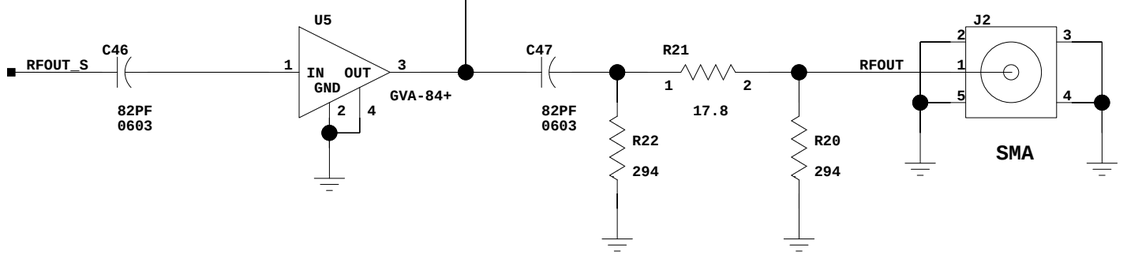












TITLE	RF AMP			
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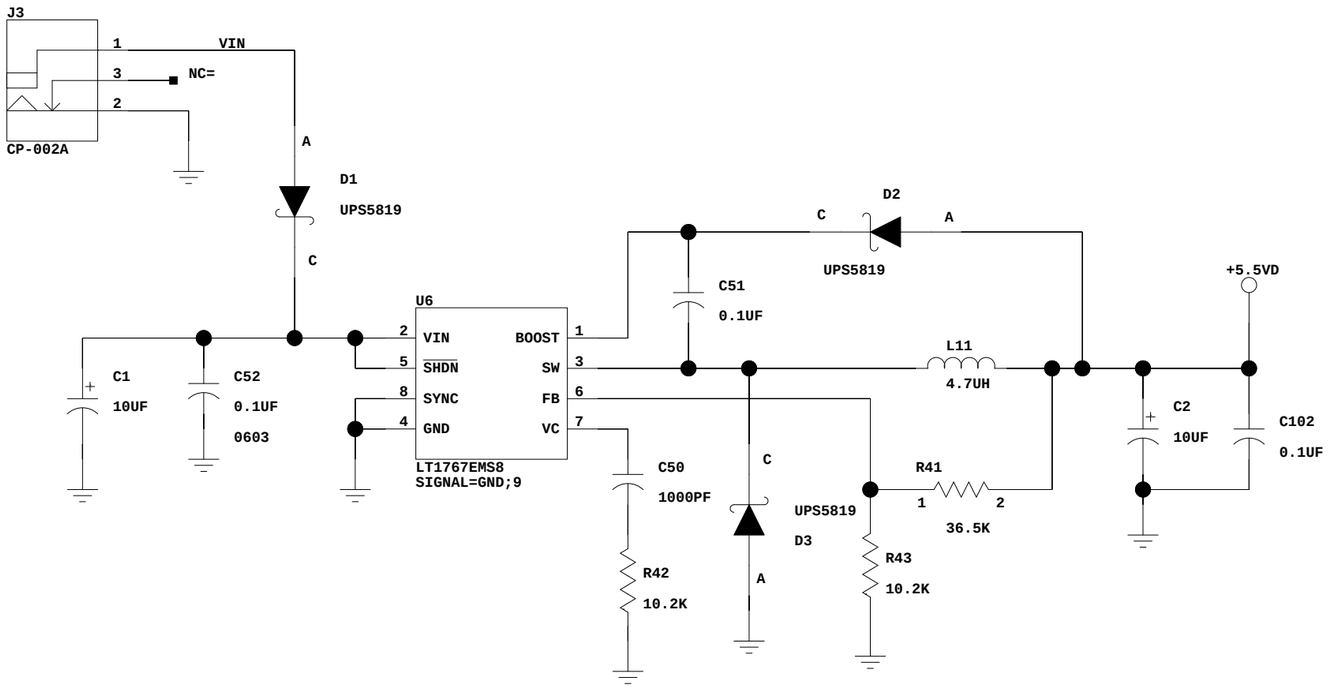

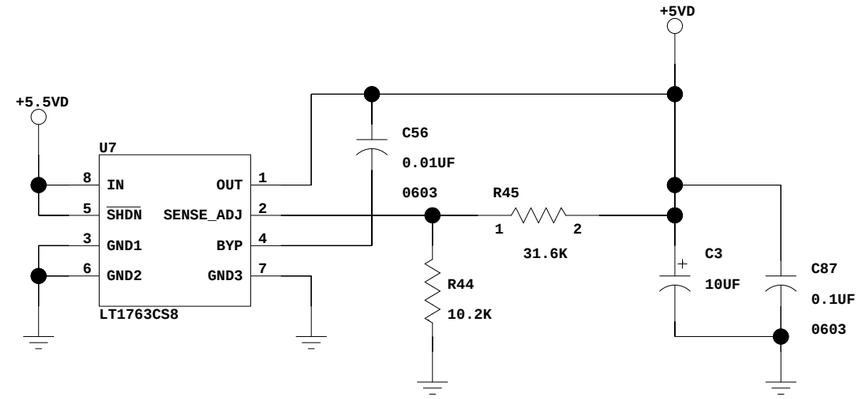

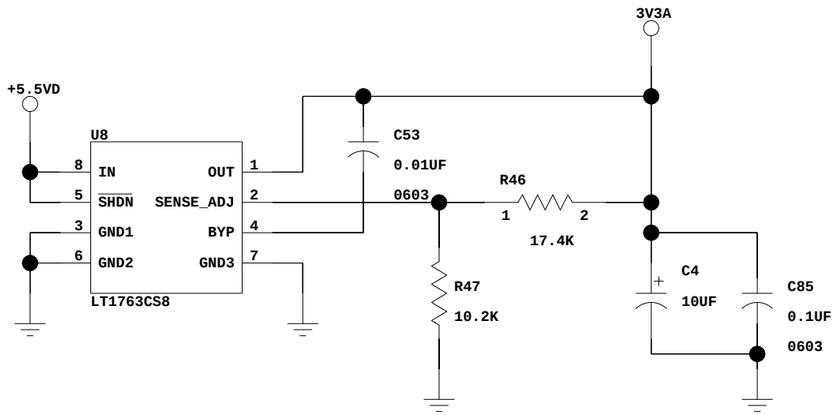

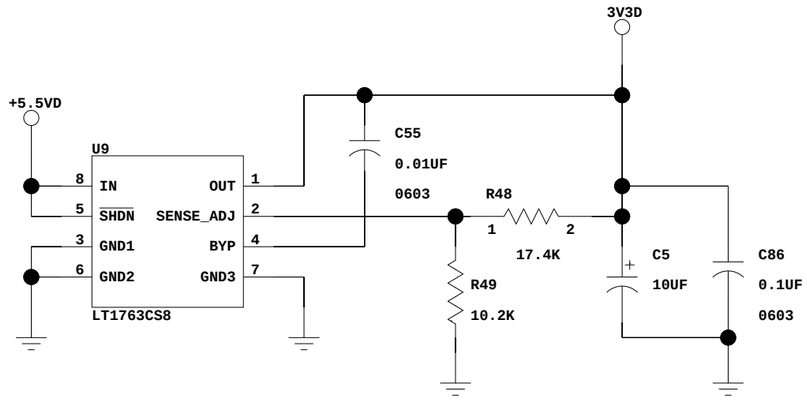

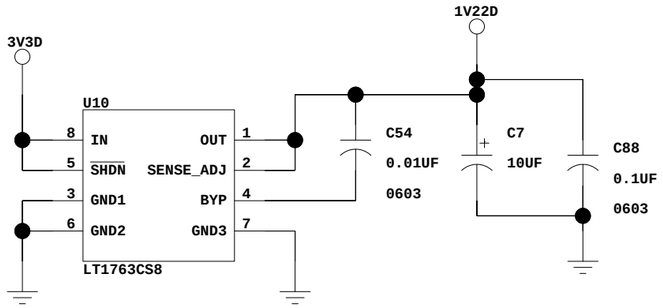

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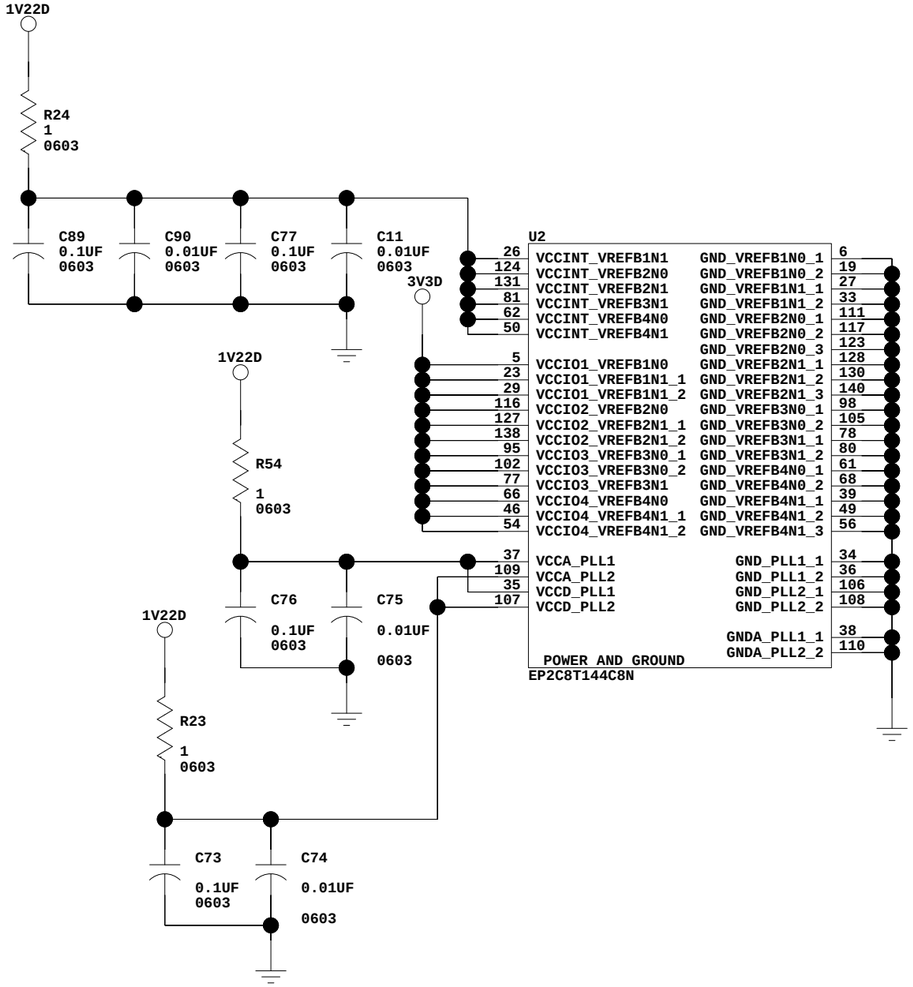

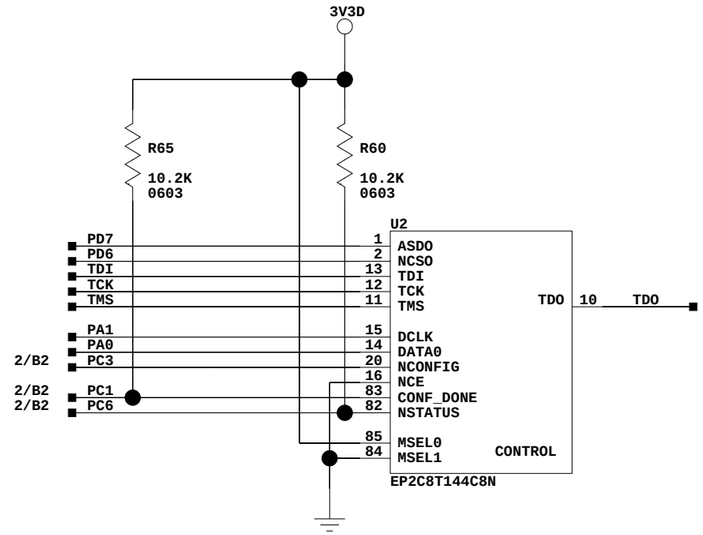

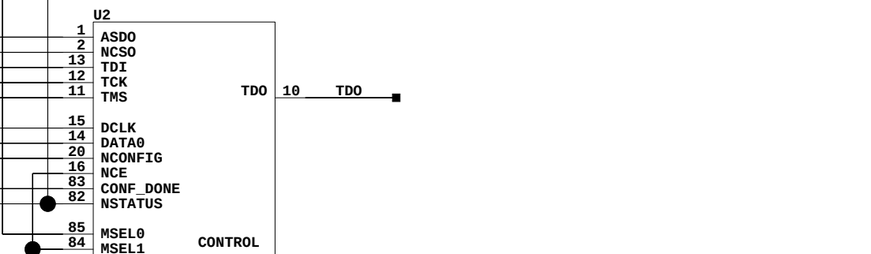

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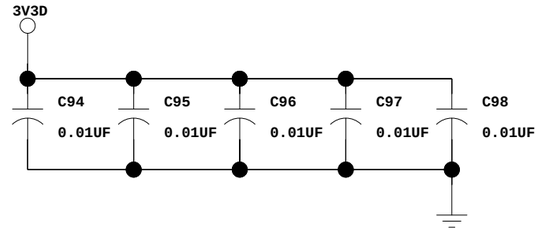

TITLE: FPGA POWER, CONTROL AND DECOUPLING CAPACITORS				
SIZE: B	DATE: 26/08/2013:19:19	FILENAME: DATV_EX	DRAWING NUMBER: 11002-001	REV: E
ENGR:			SHEET 6 OF 6	